Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**S**

**G**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .006” X .006” min.**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .036” X .036” DATE: 4/27/23**

**MFG: SUPERTEX THICKNESS .012” P/N: TN1504ND**

**DG 10.1.2**

#### Rev B, 7/19/02